Please cancel claims 8-11, 21 and 22, without prejudice.

Please add the following claims.

Claims 1-22, previously cancelled without prejudice.

Claims 23-30 now cancelled without prejudice.

31. (Amended) A phase lock loop for providing an output signal with a desired characteristic frequency that is an integer, N, multiple of a characteristic frequency of an input signal, said phase lock loop comprising:

a voltage controlled oscillator generating one or more oscillator signals, wherein each of the one or more oscillator signals are associated with M phases of the desired characteristic frequency of the output signal; [and]

a phase detector for comparing a phase or the frequency characteristic of the input signal to a phase or frequency characteristic of a particular one of the one or more oscillator signals to the input signal; and

a multiplexer for selecting a particular one of the one or more oscillator signals based on a Gray Code.

32. (Amended) The phase lock loop of claim 31, further comprising:

[a multiplexer for selecting an output signal from the one or more oscillator signals; and]

a divider circuit for reducing a characteristic frequency [of the output signal] of the selected one of the one or more oscillator signals to the desired characteristic frequency.

Claims 33 and 34 now cancelled without prejudice.

35. (Amended) The phase lock loop of claim 32 [33], further comprising:

one or more divider circuits for reducing the [frequency of the output signal to the desired] characteristic frequency [,] of at least one of the one or more oscillator signals [wherein the divider circuit reduces the frequency of the output signal by an integer, M, factor].

Cmt E'

36. (Previously Added) The phase lock loop of claim 35, [further comprising:] wherein the one or more divider circuits [for reducing the characteristic frequency of the particular one of the oscillator signals] reduce the frequency characteristic of the at least one of the one or more oscillator signals by an integer, M, factor and an integer, N, factor.

37. (Previously Added) The phase lock loop of claim 31, further comprising:

a loop filter for increasing or decreasing a characteristic frequency of the voltage controlled oscillator signals based on the comparison of the phase or frequency characteristic of the input signal to the phase or frequency characteristic of the particular one of the one or more reference clock signals by the detector.

Claim 38 is now canceled without prejudice.